

CLAIMS

What is claimed is:

- 1 1. A method comprising:
2 selectively enabling or disabling outputs of voltage regulator controllers in an electronic
3 appliance based at least in part on settings stored in non-volatile memory.
- 1 2. The method of claim 1, wherein the settings stored in non-volatile memory comprise a
2 series of delay times assigned to voltage regulator controllers.
- 1 3. The method of claim 1, wherein the outputs of the voltage regulator controllers provide
2 operating voltages to one or more components selected from the group consisting of a
3 microprocessor, a chipset, a memory controller, a graphics controller, a system memory, an
4 input/output (I/O) controller and an I/O device.
- 1 4. The method of claim 1, wherein the non-volatile memory comprises at least one memory
2 selected from the group consisting of read only memory (ROM), flash memory, battery-backed
3 static random access memory (SRAM), and electrically erasable programmable ROM
4 (EEPROM).
- 1 5. The method of claim 1, further comprising locking out a power supply until the voltage
2 regulator controller outputs are stable.

1 6. The method of claim 1, further comprising retrieving delay times for a future power state
2 change.

1 7. An electronic appliance, comprising:
2 a power supply;
3 an electronic circuit board coupled with the power supply; and
4 a sequencer engine coupled with the electronic circuit board, the sequencer engine to
5 sequentially enable voltage regulator controllers on the electronic circuit board during a power
6 up based at least in part on settings stored in non-volatile memory.

1 8. The electronic appliance of claim 7, further comprising:
2 the sequencer engine to retrieve delay times for a future power state change.

1 9. The electronic appliance of claim 7, further comprising:
2 the sequencer engine to sequentially disable voltage regulator controllers on the
3 electronic circuit board during a power down based at least in part on settings stored in non-
4 volatile memory.

1 10. The electronic appliance of claim 7, further comprising:
2 the sequencer engine to lock out the power supply until the voltage regulator controller
3 outputs are stable.

1 11. A storage medium comprising content which, when executed by an accessing machine,
2 causes the accessing machine to selectively enable or disable outputs of voltage regulator
3 controllers based at least in part on settings stored in non-volatile memory.

1 12. The storage medium of claim 11, wherein the settings stored in non-volatile memory
2 comprise a series of delay times assigned to the voltage regulator controllers.

1 13. The storage medium of claim 11, wherein the outputs of the voltage regulator controllers
2 provide operating voltages to one or more components selected from the group consisting of a
3 microprocessor, a chipset, a memory controller, a graphics controller, a system memory, an
4 input/output (I/O) controller and an I/O device.

1 14. The storage medium of claim 11, further comprising content which, when executed by
2 the accessing machine, causes the accessing machine to lock out a power supply until the voltage
3 regulator controller outputs are stable.

1 15. The storage medium of claim 11, further comprising content which, when executed by
2 the accessing machine, causes the accessing machine to retrieve delay times for a future power
3 state change.

1 16. An apparatus, comprising:
2 a non-volatile memory interface;
3 a power supply interface;

4 a voltage regulator controller interface; and
5 control logic coupled with the non-volatile memory, power supply and voltage regulator
6 controller interfaces, the control logic to retrieve delay times from non-volatile memory and to
7 enable voltage regulator controller outputs at expiration of associated delay times in response to
8 a power up request.

1 17. The apparatus of claim 16, further comprising control logic to disable voltage regulator
2 controller outputs at expiration of associated delay times in response to a power down request.

1 18. The apparatus of claim 16, further comprising control logic to retrieve ramp rate settings
2 from non-volatile memory and to set voltage regulator controller output ramp rates.

1 19. The apparatus of claim 16, further comprising control logic to retrieve delay times for a
2 future power state change.